PMICRO
Powerlink Microelectronics

PL51WT020

ADC/Touch Key
Low Power High Performance
2.4GHz RF SOC

Product Description:

PL51WT020 is an optimized true low power high performance 2.4GHz wireless system-on-chip (SOC) solution with data rates up to 1Mbps built with low bill-of-material cost, which is designed for operation in the world wide ISM frequency band at 2.400~2.4835GHz. With the flexible configurable options integrated, PL51WT020 offers a reliable and easy way of implementing touch keys, ADC, multi-function combinations for their product applications.

PL51WT020 combines the excellent performance of a leading 2.4GHz RF transceiver with a single-cycle enhanced 8051 compliant CPU, 4KB in-system programmable flash memory, 128B EEPROM data memory, 256B RAM, up to 15 General-Purpose I/O pins and many other powerful features.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

It also support address and data check out; FEC, CRC function; and Auto-Ack & Auto-Resend function.

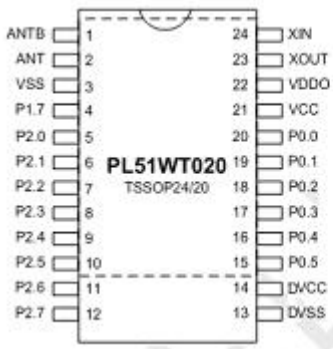
The output power of the chip can be set up to 5.5dBm and the receive sensitivity can achieve -88dBm.

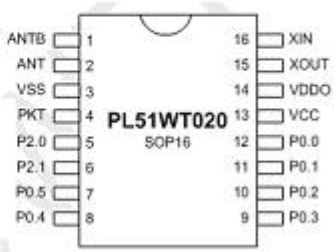
The 680K resistor and two 15pF capacitances are built in for 12MHz RF Crystal Oscillator.

The 10K pull-down resistor is built in for ANT and ANTB antenna.

PL51WT020 is communicating with the outside world with UART, I2C and SPI interfaces.

Pin Configuration:





Key Features:

- 2.4GHz RF SOC with Touch Key
- 1T Enhanced 8-Bit ET8051
- 4KB Flash and 128B EEPROM
- Data Rate over the Air：1Mbps
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-Ack and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Support HFSS
- 12MHz RF Crystal Oscillator
- Support Micro-Strip Inductor and Two Layer PCB Boards
- Fully integrated up to 9+4(shift) touch keys
- CPU Operation Freq.@Voltage:
  ~4MHz@2.0~3.6V;
  ~8MHz@2.4~3.6V;
- Operation Temperature: -40℃ ~+105℃
- Up to 15 bidirectional GPIO
- Three 16-bit Timers/Counters
- Four 12-bit PWM: PWM0/1/2/3
- Support UART/SPI/I2C interface
- Integrated 11-bit 8 channels ADC
- Package: SOP16, TSSOP20/24, SSOP24, QFN24
- Flash Cycling: 100K @25℃
- EEPROM Cycling: 500K @25℃
- Data retention: 40 years @25℃

Applications:

- Proprietary 2.4GHz Systems
- Wireless Mice, Keyboards and Game Controllers
- RF Remote Controller
- Home and Commercial Automation

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Product Types

Product Name	Package	Program Flash	Data EEPROM*5	RAM	Timer	PWM	Freq@Voltage	I/O	Interface UART/SPI/I2C	ACMP	T.S.	Touch Key*1 /Wakeup(Max)	ADC*1
Touch Key with RF Series													
PL51WT020T24	TSSOP24	4KB	128B	256B	3	4+1	~ 4M@2.0~3.6V ~ 8M@2.4~3.6V	15	1/1/1	1*4	1	9+4*3/9	11b/8ch
PL51WT020B24	SSOP24												
PL51WT020N24	QFN24	4KB	128B	256B	3	4+1		14	1/1/1	1*4	1	8+3*3/8	11b/8ch
PL51WT020T20	TSSOP20	4KB	128B	256B	3	4+1		13	1/1/1	1*4	1	7+4*3/5+4	11b/6ch
PL51WT020S16	SOP16	4KB	128B	256B	3	4+1		8	1/1/1	-	1	2+4*2/6	11b/2ch

Note: *1: Touch Key can't work with ADC at the same time, but can be set to work separately at different time slice.

*2: Shift Touch Keys <15:12> can be assigned as the touch keys <15:12> with wake-up function.

*3: Shift touch keys <15:12> or Original ones can be set to work separately at different time slice. Only Shift touch keys <15:12> or Original ones can be assigned as wake-up keys, separately.

*4: ACMP source, only between CMP1 and INTVREF (1.2V).

*5: In order to ensure that the Data EEPROM can be programmed stably, the LVR needs to be enabled and set to work greater than or equal to 2.4V(≥).

Contents

1 Overview

PL51WT020 is an optimized true low power high performance 2.4GHz wireless system-on-chip (SOC) solution with data rates up to 1Mbps built with low bill-of-material cost, which is designed for operation in the world wide ISM frequency band at 2.400~2.4835GHz. With the flexible configurable options integrated, PL51WT020 offers a reliable and easy way of implementing touch keys, ADC, multi-function combinations for their product applications.

PL51WT020 combines the excellent performance of a leading 2.4GHz RF transceiver with a single-cycle enhanced 8051 compliant CPU, 4KB in-system programmable flash memory, 128B EEPROM data memory, 256B RAM, up to 15 General-Purpose I/O pins and many other powerful features.

PL51WT020 also supports three low power modes, idle mode, stop mode and sleep mode, to reduce power consumption. With on chip regulator and advanced power management function, the current consumption in sleep mode can be reduced to nearly 2uA.

PL51WT020 has efficient power modes with RAM retention, making it highly suited for low-duty-cycle systems where ultra low power consumption is required. Short transition times between operating modes further ensure low energy consumption.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

All of the Output Power, Channel Selection, and Protocol of RF block can be configured through SPI Interface by ET8051 core.

With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

It also support address and data check out; FEC, CRC function; and Auto-Ack & Auto-Resend function.

The output power of the chip can be set up to 5.5dBm and the receive sensitivity can achieve -88dBm.

The 680K resistor and two 15pF capacitances are built in for 12MHz RF Crystal Oscillator.

The 10K pull-down resistor is built in for ANT and ANTB antenna.

PL51WT020 internal integrates high precision RC oscillator to operate and switch dynamically between a range of operating modes using different clock sources to optimize microcontroller operation and minimize power consumption.

Special algorithms are employed to reduce the possibility of false detections, increasing the touch switch application reliability under adverse environmental conditions. With auto-calibration, low operating current and low power one-key operating state, PL51WT020 provides a simple and effective means of implementing touch switches in a wide range of applications.

With integrating up to 9+4(shift) flexible touch keys (which including 4 touch keys could be shift from P2.7~P2.4 to P0.0~P0.3), PL51WT020 offers the customers a reliable and easy way of implementing touch keys for the product applications.

For high reliability and low cost issues, PL51WT020 builds in reliable watchdog timer (WDT) low power detect and low voltage reset (LPD/LVR) function.

PL51WT020 is communicating with the outside world with UART, I2C and SPI interfaces.

For easy usage, POWERLINK provides the debugger and writer.

To facilitate programming and verification, the Flash memory inside the PL51WT020 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

PL51WT020 is targeting at the proprietary 2.4GHz systems such as Human Interface Devices, Wireless Mice, Keyboards and Game Controller, RF Remote Controller, Home and Commercial Automation and etc.

2 Features

RF

- True Low Power High Performance Single Chip 2.4GHz Transceiver
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-Ack and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Data Rate over the Air：1Mbps
- Support HFSS
- Support Micro-Strip Inductor and Two Layer PCB Boards
- Built-in 680K resistor and two 15pF CAP for 12MHz RF Crystal Oscillator
- Built-in 10K pull-down resistor for ANT and ANTB antenna

Basic

- 1T 8-bit ET8051 compatible with MCS-51
- Fully integrated up to 9+4(shift) touch key functions with no external components
- CPU core Operation Frequency@Voltage: ~4MHz@2.0~3.6V; ~8MHz@2.4~3.6V
- Operation Temperature: -40℃ to +105℃
- CPU core Oscillator Type:
  - ✧ Crystal Oscillator: 400KHz to 8MHz
  - ✧ Internal RC Oscillator: 4/8MHz (±2%) and 32KHz
  - ✧ External Clock: ~8MHz
- Up to 15 bidirectional General Purpose I/O
  - ✧ Input-Only with configurable pull high resistor
  - ✧ Push-Pull Output Drive Capacity: 10mA (@3V, Total: <100mA)

Peripheral Features

- Four Priority Levels with 14 interrupt sources
  - ✧ Two External Interrupt: INT0B and INT1B
  - ✧ T0&T1 Overflow Interrupt
  - ✧ T2 Overflow, Reload, Compare/Capture Interrupt
  - ✧ UART Transmit and Receive Interrupt
  - ✧ EEPROM Write Finished Interrupt
  - ✧ Analog Comparator Interrupt
  - ✧ Keyboard Interrupt
  - ✧ Touch Key Interrupt
  - ✧ SPI Interrupt
  - ✧ I2C Interrupt
  - ✧ ADC Finish Converting Interrupt
- POR/LVR/LPD support
- Two LVR threshold Level by Fuse: 2.1/2.4V
- LPD threshold Level by Fuse: 2.7V

- Register Timed Access Protection
- Programmable System Clock
- Multi-mode Operation: Normal/Idle/Stop/Sleep
- 16-bit Timers/Counters:
  - ✧ 80C51-like Timer 0 & 1
  - ✧ 8052-like Timer 2 with Compare/Capture Unit (CCU)
- Four 12-bit PWM: PWM0/1/2/3
- Watchdog Timer with Additional Configurable Prescaler: WDT
- UART/SPI/I2C Interface
- Analog Digital Converter: ADC
  - ✧ 11-bit resolution
  - ✧ Up to 8 multiplexed channels
  - ✧ support external input VREF
- Analog Comparator: ACMP
- Support In-Circuit Programming: ICP
- ESD: >2KV (HBM)
- EFT: >4KV
- Package Types: SOP16, TSSOP20/24, SSOP24, QFN24

Memory

- 4K bytes Program Flash
- 128 bytes Data EEPROM （byte/page operation, 1page=32bytes)
- 256 bytes internal scratch-pad RAM
- Memory Programming Permission Control
- Flash Cycling: 100K @25℃
- EEPROM Cycling: 500K @25℃
- Data retention: 40 years @25℃

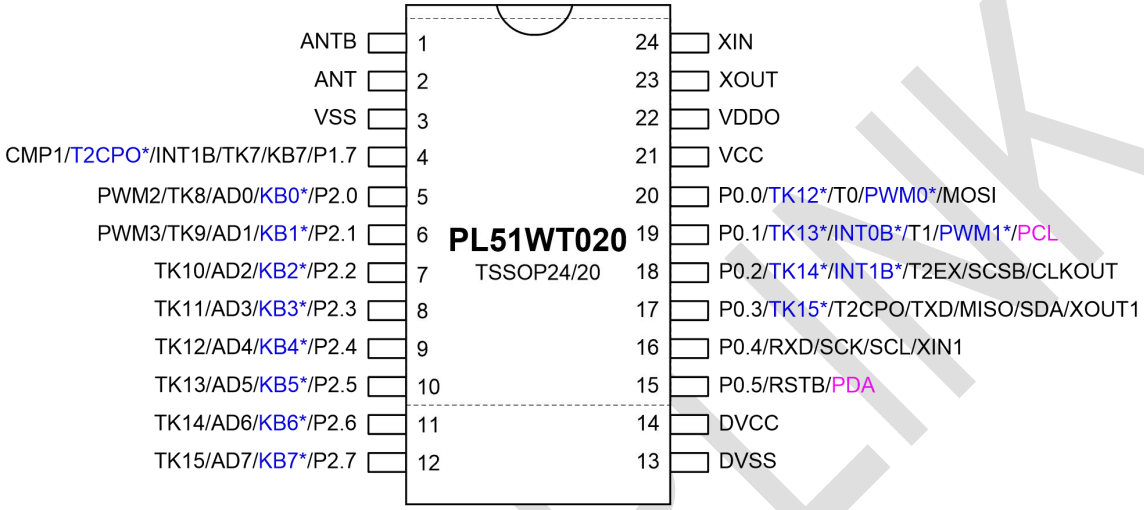
3 Quick Reference Data

Parameter	Value	Units
Min Supply Voltage	2.0	V
Max Output Power	5.5	dBm
Data Rate	1	Mbps
Current Consumption (0dBm) @TX Mode	16	mA
Current Consumption @RX Mode	17	mA
Operating Temperature Range	-40 to +105	℃
RX Sensitivity	-88	dBm
RF Crystal Oscillator	12	MHz
Internal RC OSC Frequency@25℃	4/8	MHz
Internal RC OSC Precision@25℃	±2	%
Current Consumption @ Sleep Mode	2	uA

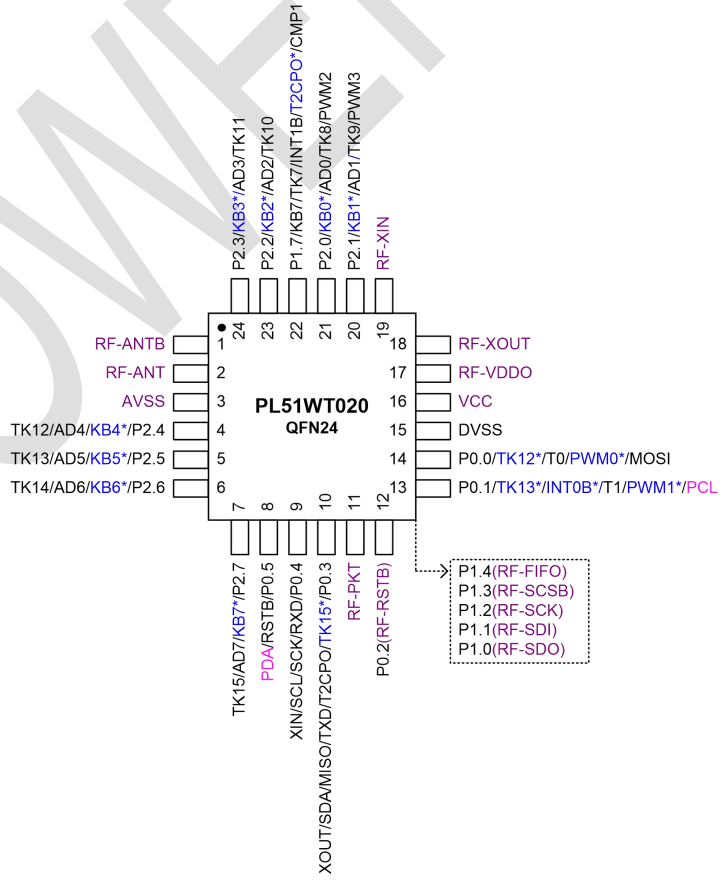
4 Pin Configurations

4.1 Pin Diagrams

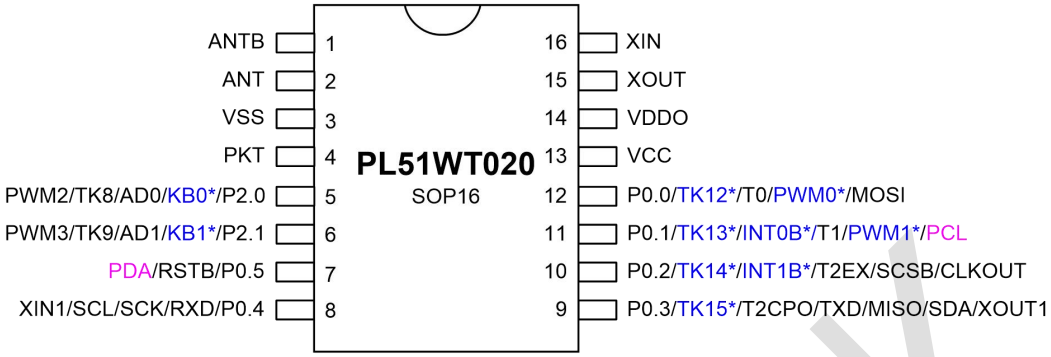
The pin map is shown as below for TSSOP24/20&SSOP24 pins.



The pin map is shown as below for QFN24 pins.



The pin map is shown as below for SOP16 pins.



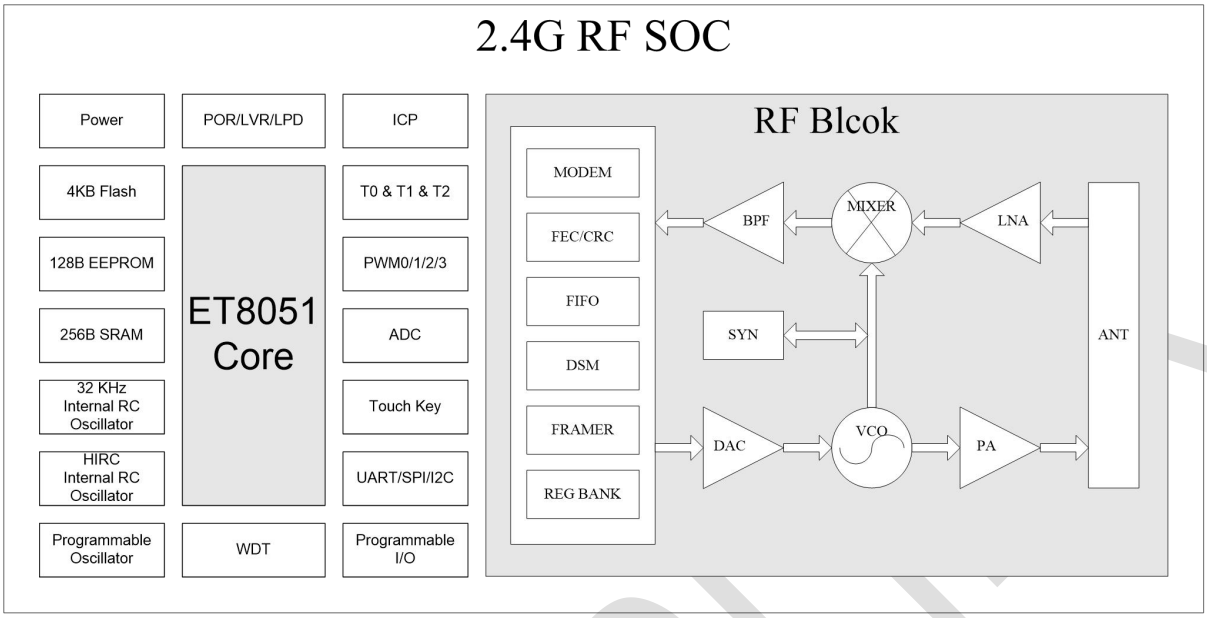
Note: *The outside pin function has the highest priority, and the inner pin function has the lowest priority. It means that if the higher priority function is enabled, the lower priority function can't be used even when the lower priority function is also enabled. The pin name colored blue with * denoted the shift ports, the pin function available only when the relative shift control bit in SFR "PSFT0~1" is set.*

4.2 Pin Description

Classify	Symbol	Type	Descriptions
Power	VCC	Power	Power Supply (2.0~3.6V)
	VSS	Power	Ground (0V)
	DVCC	Power	Power Supply (2.0~3.6V)
	DVSS	Power	Ground (0V)
	VDDO	Power	1.8V power output, connect to capacitor
RF Block	ANTB	RF	Antenna Interface
	ANT	RF	Antenna Interface
	XIN	Analog Input	12MHz Crystal Oscillator Input of RF
	XOUT	Analog Output	12MHz Crystal Oscillator Output of RF
	PKT	Digital Output	Transmit/Receive Packet Status Indicator Bit
RF Block Interface	P1.0	Digital Input	Interface of RF block SPI.SDO output
	P1.1	Digital Output	Interface of RF block SPI.SDI input
	P1.2	Digital Output	Interface of RF block SPI.SCK input
	P1.3	Digital Output	Interface of RF block SPI.SCSB input
	P1.4	Digital Input	Interface of RF block FIFO Flag output FIFO Status Indicator Bit
	P1.5	Digital Output	Interface of RF block RSTB input (Note: P0.2 is used as RF-RSTB in the QFN24)
	P1.6	Digital Input	Interface of RF block PKT Flag output Transmit/Receive Packet Status Indicator Bit (Note: RF-PKT is an independent pin in the QFN24)
Ext Reset	RSTB	Digital Input	Reset Pin of CPU core, Active Low
Clock	XIN1	Analog Input	Crystal Oscillator Input of CPU core
	XOUT1	Analog Output	Crystal Oscillator Output of CPU core
	CLKOUT	Digital Output	Internal Clock Output of CPU core
UART	RXD	Digital Input	RXD of Serial Port
	TXD	Digital Output	TXD of Serial Port
SPI	SCSB	Digital Input	Enable Input for SPI Interface, active Low
	SCK	Digital I/O	Clock for SPI Interface
	MISO	Digital I/O	Master Data Input or Slave Data Output for SPI Interface

Classify	Symbol	Type	Descriptions
	MOSI	Digital I/O	Master Data Output or Slave Data Input for SPI Interface
I2C	SCL	Digital I/O	Clock for I2C Interface
	SDA	Digital I/O	Data I/O for I2C Interface
Timer0	T0	Digital Input	Timer 0 Input
Timer1	T1	Digital Input	Timer 1 Input
Timer2	T2 EX	Digital Input	Timer 2 external reload or gate Input
	T2CPO	Digital Output	T2 compare or PWM output
Ext Interrupt	INT0B	Digital Input	External Interrupt 0
	INT1B	Digital Input	External Interrupt 1
PWM	PWM0	Digital Output	PWM 0 Output
	PWM1	Digital Output	PWM 1 Output
	PWM2	Digital Output	PWM 2 Output
	PWM3	Digital Output	PWM 3 Output
ACMP	CMP1	Analog Input	Comparator channel 1 Input
ADC	AD0~7	Analog Input	8 channels AD Input
Touch Key	TK7~15	Analog Input	9 channels Touch Key Inputs
Key Board	KB0~7	Analog Input	8 channels Keyboard Inputs
PORT0	P0.0~P0.5	Digital I/O	General purpose I/O Port 0
PORT1	P1.7	Digital I/O	General purpose I/O Port 1
PORT2	P2.0~P2.7	Digital I/O	General purpose I/O Port 2
ICP	PCL	Digital Input	Clock Input for ICP/ICD Mode
	PDA	Digital I/O	Data I/O for ICP/ICD Mode

5 Block Diagram



6 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage and affect device reliability if exceeded.

Parameter	Symbol	Value	Units
Supply Voltage of VDD	VDD	-0.3 to +3.6	V
Supply Voltage of VCC	VCC	-0.3 to +3.6	V
Supply Voltage of VDDO	VDDO	-0.3 to +2.5	V
Input Voltage	V_{IN}	-0.3 to (VDD+0.3)	V
Operating Temperature	T_{OP}	-40 to +105	℃
Storage Temperature	T_{ST}	-55 to +150	℃
Maximum Current into VDD	/	100	mA
Maximum Current out of VSS	/	100	mA
Maximum Current suck by a I/O pin	/	10	mA
Maximum Current sourced by a I/O pin	/	10	mA
Maximum Current suck by total I/O pins	/	100	mA
Maximum Current sourced by total I/O pins	/	100	mA

Note: *These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.*

7 Electrical Characteristics

7.1 RF Electrical Characteristics

(Conditions：VCC=+3V，VSS=0V，TA=－40℃ to +105℃)

Symbol	Parameter (Condition)	Notes	Min.	Typ.	Max.	Units
	Operating Conditions					
VCC	Supply voltage of VCC		2.0	3.3	3.6	V
T_{OP}	Operating Temperature		-40		105	℃
	General RF Conditions					
f_{OP}	Operating frequency		2402		2480	MHz
f_{XTAL}	Crystal Frequency			12		MHz
$\triangle f_{1M}$	Frequency Deviation @1Mbps			280		KHz
R_{GFSK}	Data Rate			1		Mbps
$F_{CHANNEL}$	Channel Spacing			1		MHz
	Transmitter Operation					
P_{RF}	Maximum Output Power			0	5.5	dBm
P_{RFC}	RF Power Control Range		18	20	22	dB
P_{RF1}	1st Adj. Channel TX Power				-20	dBm
P_{RF2}	2nd Adj. Channel TX Power				-50	dBm
I_{VCC_H}	Power Consumption @High Gain			16		mA
I_{VCC_L}	Power Consumption @Low Gain			12		mA
	Receiver Operation					
I_{VCC}	Power Consumption			17		mA
RX_{SENS}	RX Sensitivity @0.1%BER			-88		dBm

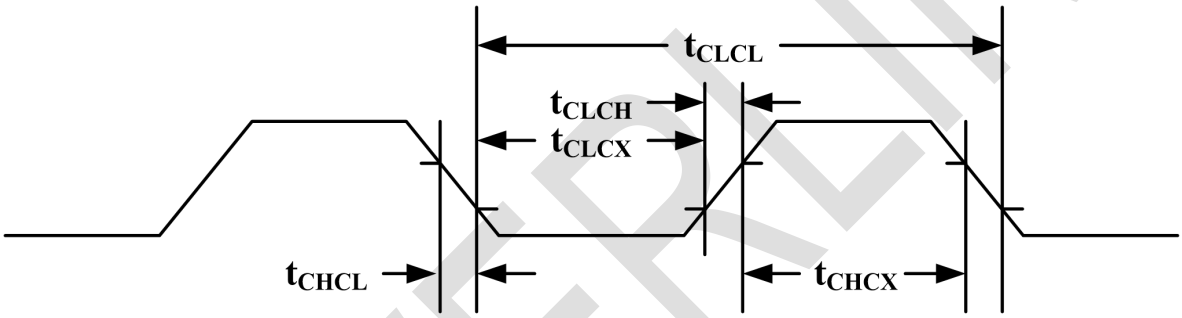
7.2 DC Electrical Characteristics

(VDD = 2.0V~3.6V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Operating Voltage	VDD	2.0	3.3	3.6	V	CPU core Freq: ~4MHz
		2.4	3.3	3.6	V	CPU core Freq: ~8MHz
Operation Current	I_{OP}		2		mA	No load, VDD=3.3V@8MHz
IDLE Current	I_{IDLE}		1		mA	No load, VDD=3.3V@8MHz, IDLE
STOP Current	I_{STOP}		5		uA	No load, VDD=3.3V, STOP
SLEEP Current	I_{SLEEP}		2		uA	No load, VDD=3.3V, SLEEP

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Input High Voltage	V_{IH}	0.7*VDD		VDD+0.2	V	
Input Low Voltage	V_{IL}	-0.5		0.3*VDD	V	
Output High Voltage	V_{OH}	2.6			V	VDD=3.3V, I_{OH}=-10mA
Output Low Voltage	V_{OL}			0.7	V	VDD=3.3V, I_{OL}=+10mA
Port Pull up Resistor	R_{PU}		50		KΩ	
POR slope rate	S_{POR}	0.025		4.5	V/ms	
POR threshold voltage of rising	V_{PORH}	0.4	0.8	1.2	V	
POR threshold voltage of falling	V_{PORL}	0.4	0.7	1.0	V	
POE threshold voltage	V_{POE}		1.4		V	

7.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

7.3.1External Clock Characteristics

(VDD = 2.0V~3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency				8	MHz	
Clock High Time	t_{CHCX}	30			ns	
Clock Low Time	t_{CLCX}	30			ns	
Clock Rise Time	t_{CLCH}			10	ns	
Clock Fall Time	t_{CHCL}			10	ns	

7.3.2Internal RC OSC Characteristics

(VDD = 2.0V~3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency			4/8		MHz	
Clock Frequency			±2		%	T_A = 25°C
Clock Frequency			±5		%	T_A = -40°C~+105°C

7.3.3Crystal Oscillator/Ceramic Resonator Characteristics

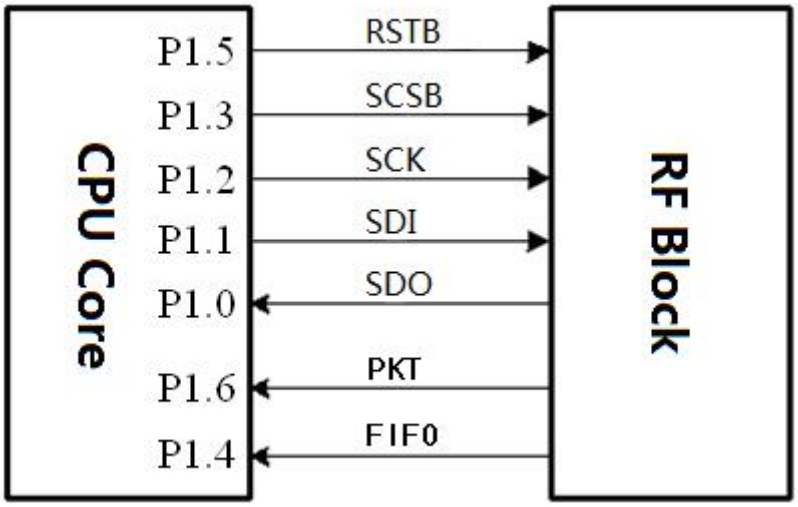
(VDD = 2.0V~3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency		400K		8M	Hz	

8 Internal RF Interface

8.1 SPI Data and Control

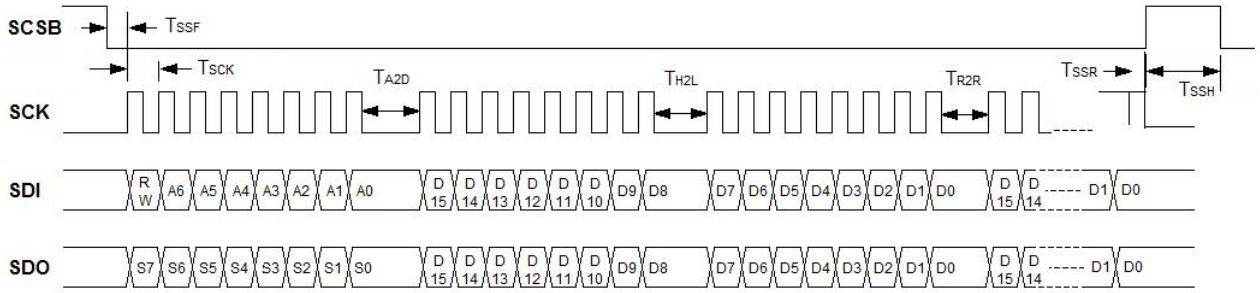
The RF block provides a simple interface for application, consisting of SPI interface plus two handshake signals. The RF block SPI supports slave mode only.



The data and control interface gives access to all the features in the chip. The data and control interface consists of the following seven digital signals:

Pin	Description
RSTB	Reset Input, active low (Note: P0.2 is used as RF-RSTB in the QFN24)
SCSB	SPI Slave Select Input Wakeup from SLEEP state
SCK	SPI Clock Input
SDI	SPI Data Input
SDO	SPI Data Output
PKT	Packet TX/RX Flag (Note: RF-PKT is an independent pin in the QFN24)
FIFO	FIFO Status Indicator Bit

8.2 SPI Command Format



Note: The device SPI bus setup data when the rising edge of the master SCK, and sample data at the falling edge of the master SCK.

Name	Min.	Typ.	Max.	Description
T_{SSH}	250ns			Interval between two SPI accesses
T_{SSF}, T_{SSR}	41.5ns			Relationship between SCSB and SCK
T_{A2D}	*1			Interval time between address and data
T_{H2L}	*1			Interval time between high byte and low byte data
T_{R2R}	*1			Interval time between two register data
T_{SCK}	83ns			SCK period

Note: *1--When reading FIFO data, at least 450ns wait time is required. Otherwise, $T3_{min}$ = 41.5ns.

9 Memory

The Memory contains 4K bytes program code Flash, 128 bytes data code EEPROM.

- 4K bytes program Flash
- 128 bytes data EEPROM

9.1 Memory Encryption

The program code area is encrypted in this device.

9.2 Register Definition

9.2.1EEPROM Control Register – EECON

Table 9- 1 EECON Register (97h)

Bit	Symbol	Description	Type	Reset
eecon.7	LOCK	**EEPROM program inhibit** 0 – EEPROM program is enabled 1 – EEPROM program is inhibited	R/W	0
eecon.6	-	-	-	0
eecon.5	-	-	-	0
eecon.4	-	-	-	0
eecon.3	EPGM	**EEPROM program interrupt enable** When epgm=0 EEPROM program interrupt is disabled. When epgm=1 and ea=1 EEPROM program interrupt is enabled.	R/W	0
eecon.2	PGMF	**EEPROM program interrupt flag** 1 – EEPROM program is finished It can only be set by hardware and can be cleared by software or interrupt. When set PGM to 1, it will be cleared automatically.	R/W	0
eecon.1	CPF	**EEPROM program cross page flag** 1 – EEPROM program page is changed (cross page) If CPF=1, PGM can not be set to 1 until CPF is cleared by software. CPF can only be set to 1 by hardware; it can not be set to 1 by software.	R/W	0

Bit	Symbol	Description	Type	Reset
		After cross page error occurred, more than 3 NOP must be followed close behind the CPF cleared instruction to avoid the reset operation of EEPROM.		
eecon.0	PGM	**EEPROM program enable** 1 – start EEPROM program After write data to EEPROM buffer, set it to start EEPROM program. If EEPROM buffer is not written, software can not set it. When program is finished, it is cleared by hardware automatically. It can not be cleared by software.	R/TW	0

10 ICP (In-Circuit Programming)

The contexts of flash in the device are empty by default. User must program the flash by external Writer device or by ICP (In-Circuit Programming) tool.

In the ICP tool, the user must take note of ICP's programming pins used in system board. In some application circuits, it is highly recommended customer power off then power on after ICP programming has completed on the system board.

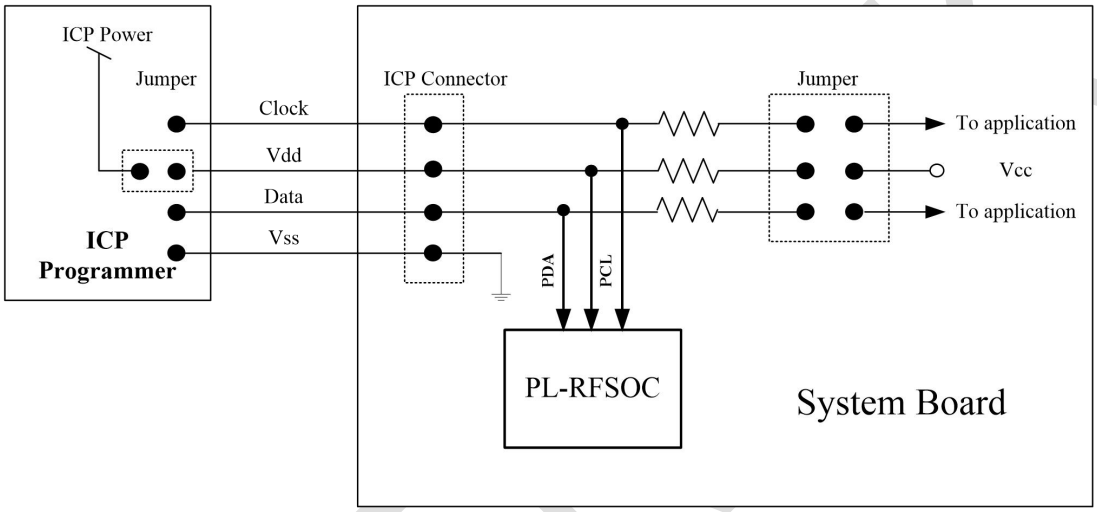


Figure 10- 1 ICP Application Circuit

Note:

1. Circuitry separation is optionally needed between ICP and application during ICP operation.
2. Resistor is optional by application
3. When using ICP to upgrade code, the clock PCL and data PDA must be taken within design system board.
4. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.

The device supports programming of Flash (4K bytes AP Flash), and data EEPROM (128 bytes). User has the option to program the AP Flash and data EEPROM either individually or both.

11 Config Options

The config options are used for code configuration.

Config Option0	Config Option1	Config Option2
Program Flash lock bit	**Reserved**	**LVR enable** 0x – disabled 10 – always enabled 11 – enabled except EE program
Data EEPROM lock bit	**Reset pin enable**	
XTAL options OPT[0]: 0 -> use inner feedback resistor 1 -> no inner feedback resistor OPT[1]: 0 -> select inner 1M resistor 1 -> select inner 4M resistor OPT[2]: 0 -> no 15pf inner cap 1 -> use 15pf inner cap	**Pump clock vision select** 0 –Not dived the pump clock 1 –Dived the pump clock by 2	**LVR threshold level** 00 – 2.1v 01 – 2.4v 10 – reserved 11 – reserved
	Clock output enable	
	Warm-up time 00~11: long warm-up time → short warm-up time	**LPD** enable
Oscillator type selection 000 – external clk input mode 001 – Internal RC 32KHz 01x – Crystal Oscillator 100 – Internal RC 4MHz 101 – Internal RC 8MHz 110 – reserved 111 – reserved		**LPD threshold level** 0 – 2.7v 1 – reserved
	Time-out delay 00 – 2112 clocks (65ms) 01 – 576 clocks (18ms) 10 – 256 clocks (8ms) 11 – 128 clocks (4ms)	**WDT enable** 0x – disabled 10 – enabled controlled by WDTEN 11 – enabled controlled by WDTEN disabled in STOP mode

12 CPU Core Information

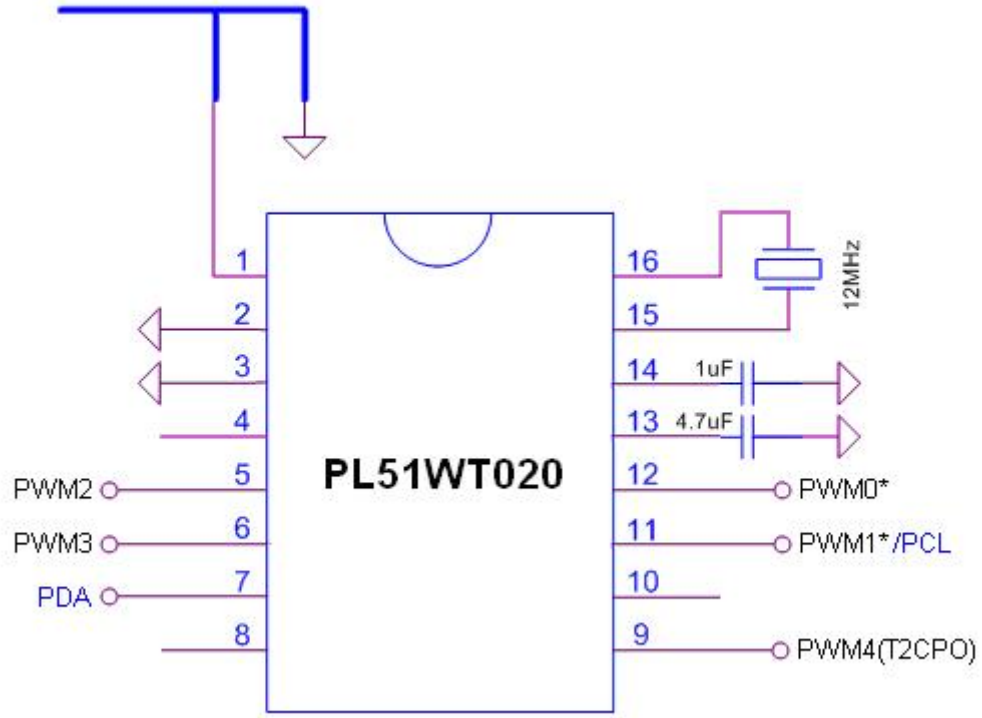
The detail description of CPU core is in user manual, please contact with POWERLINK.

13 RF Block Control Register Information

The latest recommended control registers value is in user manual, please contact with POWERLINK.

14 Typical Application

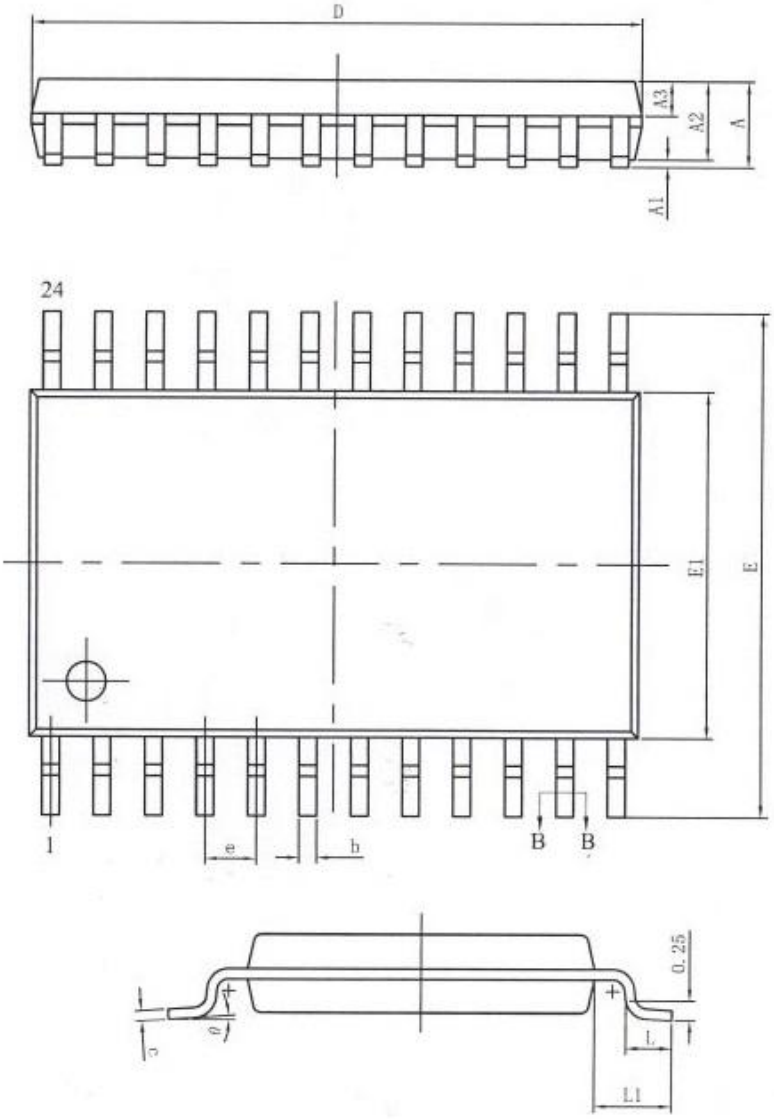
14.1 Smart Lighting: RGB+CW/WW



15 Package Dimensions

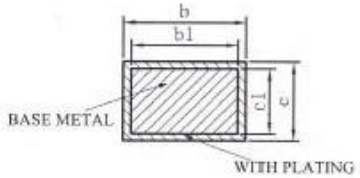
15.1 TSSOP24 Package

TSSOP24 PACKAGE OUTLINE DIMENSIONS



TSSOP24L

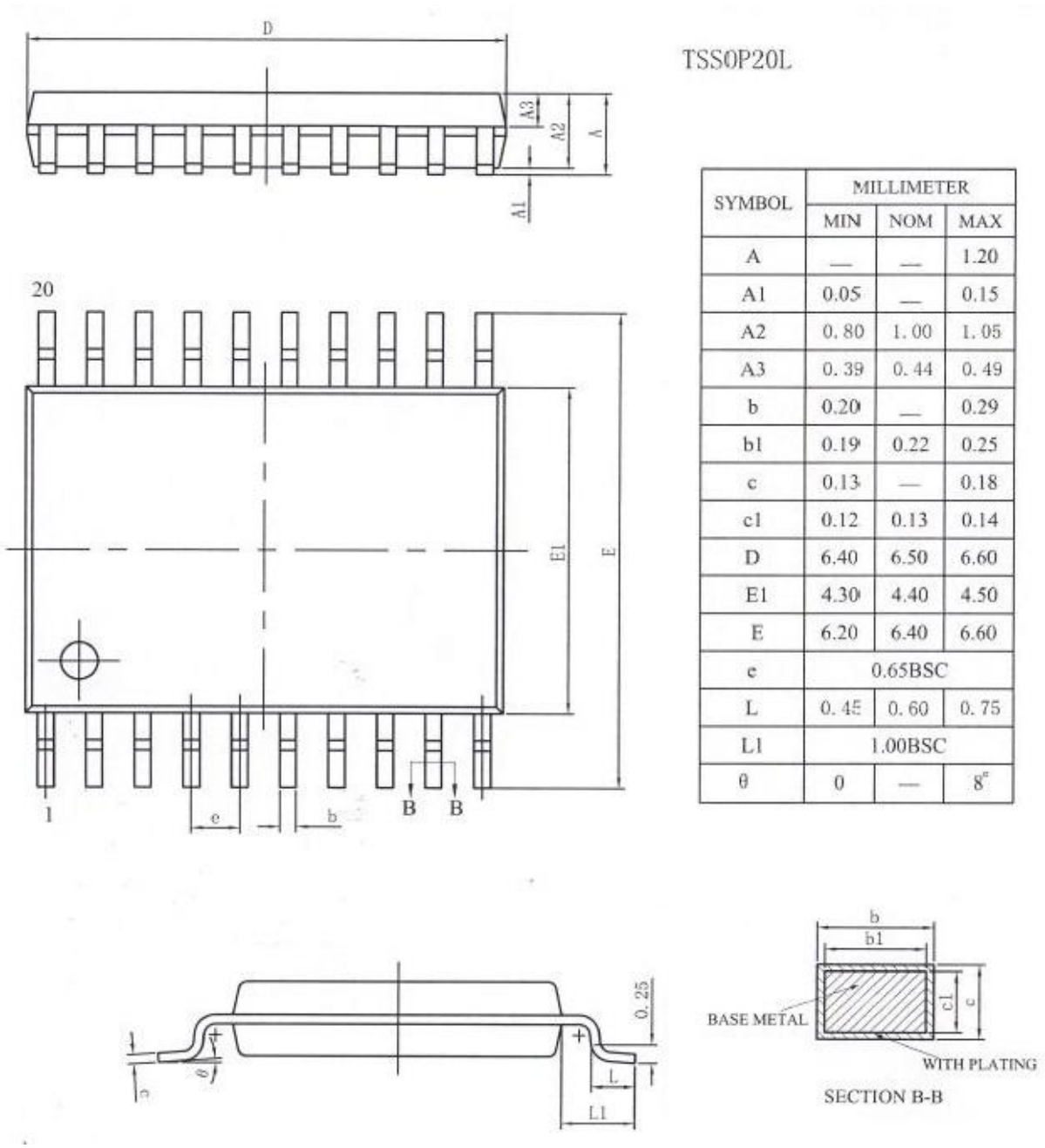
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°



SECTION B-B

15.2 TSSOP20 Package

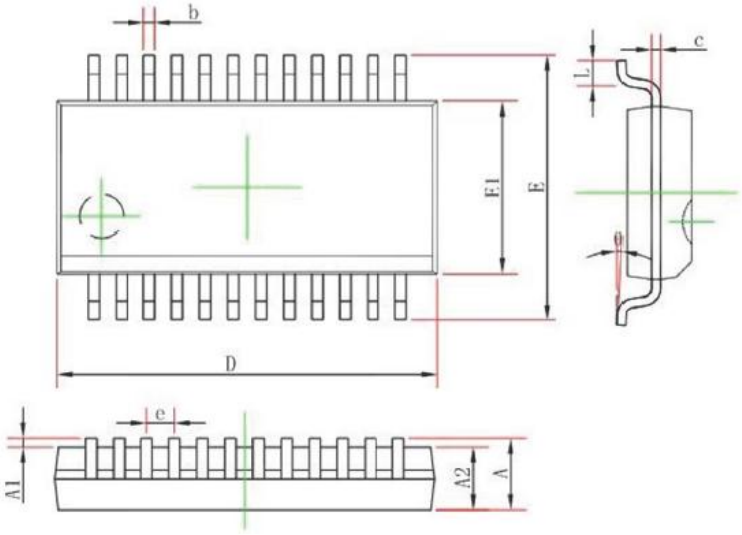
TSSOP20 PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

15.3 SSOP24 Package

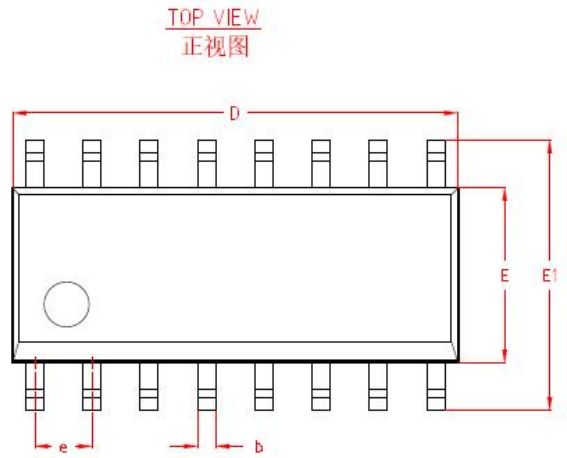
SSOP24 PACKAGE OUTLINE DIMENSIONS

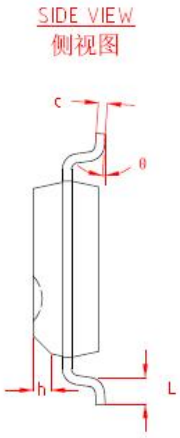


Symbol	Dimensions In Millimeters	
	Min	**Max**
A	——	1.750
A1	0.050	0.080
A2	1.400	1.500
b	0.203	0.305
c	0.102	0.254
D	8.550	8.650
E1	3.800	4.000
E	5.800	6.200
e	0.635 (BSC)	
L	0.400	1.270
θ	0°	8°

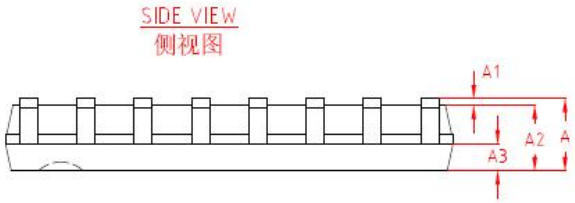
15.4 SOP16 Package

SOP16 PACKAGE OUTLINE DIMENSIONS



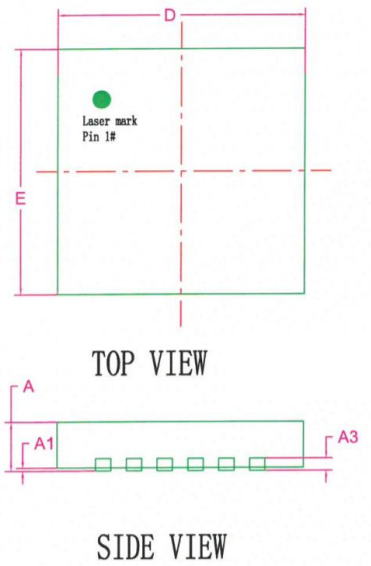


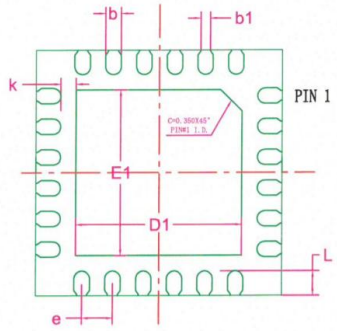
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	–	0.50
c	0.19	–	0.25
D	9.80	10.00	10.20
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	–	0.50
L	0.40	–	0.80
θ	0°	–	8°



15.5 QFN24(4*4*0.75) Package

QFN24(4*4*0.75) PACKAGE OUTLINE DIMENSIONS





Symbol	Dimensions in mm		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
A3		0.203TYP	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
⚠D1	2.60	2.70	2.80
⚠E1	2.60	2.70	2.80
k		0.20MIN	
b	0.18	0.25	0.30
b1		0.16REF	
e		0.50BSC	
L	0.35	0.40	0.45

16 Ordering Information

Part Number	Packaging
PL51WT020S16	SOP16, Tube
PL51WT020S16R	SOP16, Tape&Reel
PL51WT020T20	TSSOP20, Tube
PL51WT020T24	TSSOP24, Tube
PL51WT020B24	SSOP24, Tube
PL51WT020N24R	QFN24, Tape&Reel
……	……

17 Document Revision History

Rev.	Date	Comments
0.1	2016/11/18	Preliminary Version
0.2	2017/02/14	PL51WT020: Change Memory's description
0.3	2017/03/08	Removed TempSensor, and updated some descriptions
0.4	2017/10/10	Max Output Power: 5.5 dBm
0.5	2017/10/16	Fixed: Pin Description of SPI interface
0.6	2018/07/11	Operation Temperature
0.7	2018/10/26	Updated PACKAGE OUTLINE DIMENSIONS
0.8	2019/06/06	Added SSOP24 package
0.9	2020/04/10	Updated PACKAGE OUTLINE DIMENSIONS
1.0	2021/03/18	Updated Part Number Description
1.1	2024/03/04	Added QFN24(4*4*0.75) package

18 Important Notice

POWERLINK reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.