PL1166A

Low Power High Performance Single Chip 2.4GHz Transceiver

Product Description:

PL1166A is a piece of true low power high performance single chip 2.4GHz transceiver, which is designed for operation in the world wide ISM frequency band at 2.400~2.4835GHz.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

All of the Output Power, Channel Selection, and Protocol can be configured through SPI/I2C Interface.

With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

It also support address and data check out; FEC, CRC function; and Auto-Ack & Auto-Resend function.

The output power of the chip can be set up to 5.5dBm and the receive sensitivity can achieve -88dBm.

With on chip regulator and advanced power management function, the current consumption in sleep mode can be reduced to nearly 1uA.

The 680K resistor and two 15pF capacitances are built in for Crystal Oscillator.

The 10K pull-down resistor is built in for ANT and ANTB antenna.

The patent zero-current pull-down structure for MODE pin. After RSTB reset, SPI MODE is selected by default.

Pin Configuration:
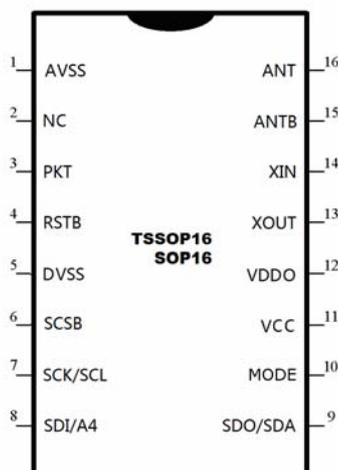
Key Features:

- True Low Power High Performance Single Chip 2.4GHz Transceiver
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-Ack and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Data Rate over the air：1Mbps
- Support HFSS
- Support Micro-Strip Inductor and Two Layer PCB Boards
- 1.9 to 3.6V supply range
- Packages: TSSOP16/SOP16
- TSSOP16/SOP16 support SPI and I2C Interface
- Built-in 680K resistor and two 15pF CAP for Crystal Oscillator
- Built-in 10K pull-down resistor for ANT and ANTB antenna
- patent zero-current pull-down structure for MODE pin

Applications:

- Wireless Mice, keyboards and Game Controllers
- Wireless Data Communication
- Wireless Door Accessing
- Wireless Networks
- Safety and Guard System
- RF Remote Control
- Remote Sensing
- Sports watches and sensors
- Home and commercial automation
- Industrial Sensors
- Industrial and Commercial Short Range Communication
- VoIP headsets
- Toys

1 Overview

PL1166A is a piece of true low power high performance single chip 2.4GHz transceiver, which is designed for operation in the world wide ISM frequency band at 2.400~2.4835GHz.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

All of the Output Power, Channel Selection, and Protocol can be configured through SPI/I2C Interface.

With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

It also support address and data check out;

FEC, CRC function; and Auto-Ack & Auto-Resend function.

The output power of the chip can be set up to 5.5dBm and the receive sensitivity can achieve -88dBm.

With on chip regulator and advanced power management function, the current consumption in sleep mode can be reduced to nearly 1uA.

The 680K resistor and two 15pF capacitances are built in for Crystal Oscillator.

The 10K pull-down resistor is built in for ANT and ANTB antenna.

The patent zero-current pull-down structure for MODE pin. After RSTB reset, SPI MODE is selected by default.

2 Features

- True Low Power High Performance Single Chip 2.4GHz Transceiver
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-Ack and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Data Rate over the air：1Mbps
- Support HFSS
- Support Micro-Strip Inductor and Two Layer PCB Boards

- 1.9 to 3.6V supply range
- Packages: TSSOP16/SOP16
- TSSOP16/SOP16 support SPI and I2C Interface
- Built-in 680K resistor and two 15pF CAP for Crystal Oscillator
- Built-in 10K pull-down resistor for ANT and ANTB antenna
- patent zero-current pull-down structure for MODE pin
- PL1166A's registers are fully compatible with PL1167 and PL1166

3 Quick Reference Data

Parameter	Value	Units
Min Supply Voltage	1.9	V
Max Output Power	5.5	dBm
Data Rate	1	Mbps
Current Consumption (0dBm) @TX Mode	16	mA
Current Consumption @RX Mode	17	mA
Operating Temperature Range	-40 to +105	℃
RX Sensitivity	-88	dBm
Current Consumption @Sleep Mode	1	uA

4 Pin Diagrams

The pin map is shown as below for TSSOP16 and SOP16.
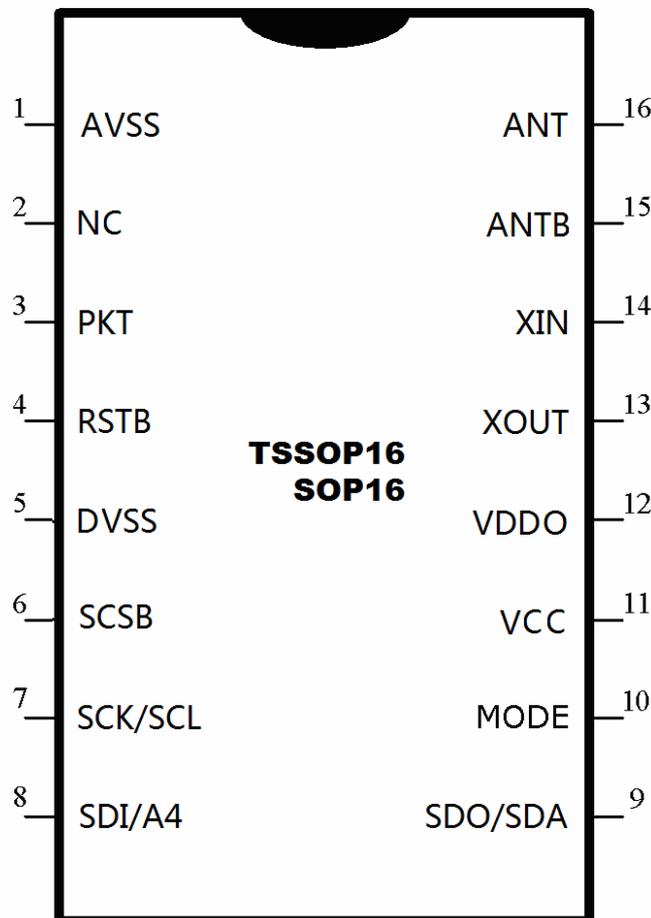
5 Pin Description

Pin	Name	Pin Function	Description
1	AVSS	Power	Ground (0V)
2	NC	N/C	Not Connected
3	PKT	Digital Output	Transmit/Receive Packet Status Indicator Bit
4	RSTB	Digital Input	Reset Pin, active low
5	DVSS	Power	Ground (0V)
6	SCSB	Digital Input	SPI: Enable Input for SPI Interface, active Low Wakeup from SLEEP state I2C: Wakeup from SLEEP state
7	SCK/SCL	Digital Input	SCK: Clock Input for SPI Interface SCL: Clock Input for I2C Interface
8	SDI/A4	Digital Input	SDI: Data Input for SPI Interface A4: Address bit 4 for I2C Interface
9	SDO/SDA	Digital Output	SDO: Data Output for SPI Interface (tri-state when not active) SDA: Data I/O for I2C interface

10	MODE	Digital Input	Mode Selection: (Patent pull-down)
			
			     VSS: Select SPI Interface
			
			     VCC: Select I2C Interface

11	VCC	Power	Power Supply (3.3V)
12	VDDO	Power	1.8V power output，connect to capacitor
13	XOUT	Analog Output	Crystal Oscillator Output
14	XIN	Analog Input	Crystal Oscillator Input
15	ANTB	RF	Antenna Interface
16	ANT	RF	Antenna Interface

6 Block Diagram
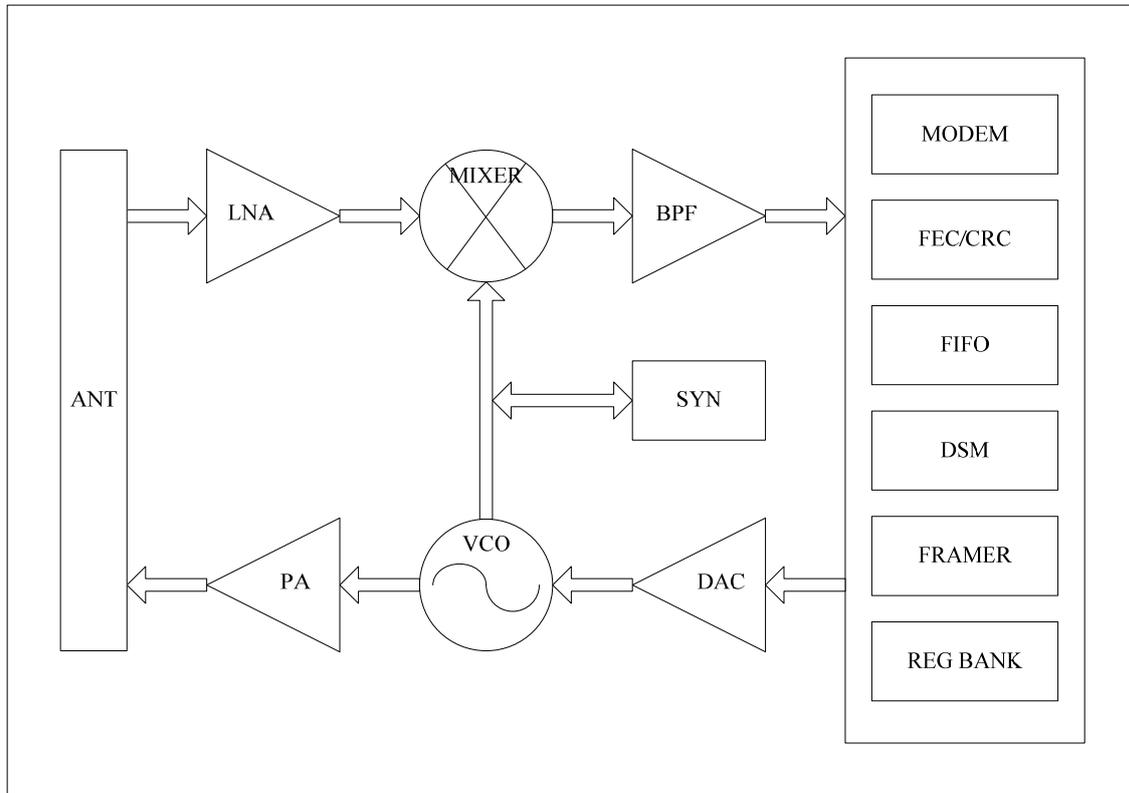
7 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage and affect device reliability if exceeded.

Parameter	Symbol	Value	Units
Supply Voltage of VCC	VCC	-0.3 to +3.6	V
Supply Voltage of VDDO	VDDO	-0.3 to +2.5	V
Input Voltage	V_{IN}	-0.3 to (VCC+0.3)	V
Output Voltage	V_{OUT}	-0.3 to (VCC+0.3)	
Operating Temperature	T_{OP}	-40 to +105	℃
Storage Temperature	T_{ST}	-40 to +125	℃

Note: These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

8 Electrical Characteristics

(Conditions：VCC=+3V，VSS=0V，TA=－40℃ to +105℃)

Symbol	Parameter (Condition)	Notes	Min.	Typ.	Max.	Units
	Operating Conditions					
VCC	Supply voltage of VCC		1.9	3.3	3.6	V
T_{OP}	Operating Temperature		-40		105	℃
	Digital Input Pin					
V_{IH}	High Level Input Voltage		0.8VCC		1.2VCC	V
V_{IL}	Low Level Input Voltage		0		0.2VCC	V
	Digital Output Pin					
V_{OH}	High Level Output Voltage		0.8VCC		VCC	V
V_{OL}	Low Level Output Voltage		0		0.2VCC	V
	General RF Conditions					
f_{OP}	Operating frequency		2402		2480	MHz
f_{XTAL}	Crystal Frequency			12		MHz
$\triangle f_{1M}$	Frequency Deviation @1Mbps			280		KHz
R_{GFSK}	Data Rate			1		Mbps
$F_{CHANNEL}$	Channel Spacing			1		MHz
	Transmitter Operation					
P_{RF}	Maximum Output Power			0	5.5	dBm
P_{RFC}	RF Power Control Range		18	20	22	dB
P_{RF1}	1st Adj. Channel TX Power				-20	dBm
P_{RF2}	2nd Adj. Channel TX Power				-50	dBm
I_{VCC_H}	Power Consumption @High Gain			16		mA
I_{VCC_L}	Power Consumption @Low Gain			12		mA
	Receiver Operation					
I_{VCC}	Power Consumption			17		mA
RX_{SENS}	RX Sensitivity @0.1%BER			-88		dBm

9 SPI Interface

9.1 SPI Data and Control

The chip provides a simple interface for application MCU, consisting of SPI interface plus two handshake signals. The chip SPI supports slave mode only.
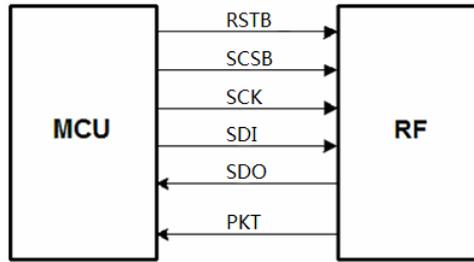
The data and control interface gives access to all the features in the chip. The data and control interface consists of the following seven digital signals:

Pin	Description
RSTB	Reset Input, active low
MODE	Mode Selection: 0—SPI, pull-down after POR
SCSB	SPI Slave Select Input Wakeup from SLEEP state
SCK	SPI Clock Input
SDI	SPI Data Input
SDO	SPI Data Output
PKT	Packet TX/RX Flag

9.2 SPI Command Format
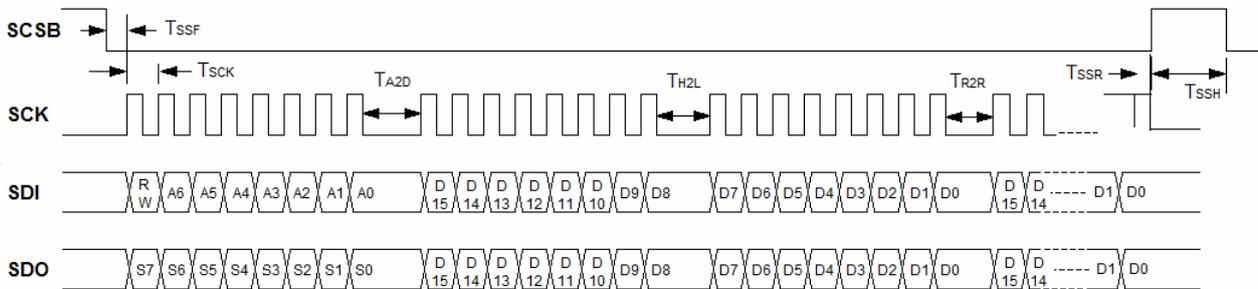
Note: The device SPI bus setup data when the rising edge of the master SCK, and sample data at the falling edge of the master SCK.

Name	Min.	Typ.	Max.	Description
T_{SSH}	250ns			Interval between two SPI accesses
T_{SSF}, T_{SSR}	41.5ns			Relationship between SCSB and SCK
T_{A2D}	*1			Interval time between address and data
T_{H2L}	*1			Interval time between high byte and low byte data
T_{R2R}	*1			Interval time between two register data
T_{SCK}	83ns			SCK period

Notes: *1--When reading FIFO data, at least 450ns wait time is required. Otherwise, $T3_{min} = 41.5ns$.

10 I2C Interface

10.1 I2C Data and Control

Pin	Description
RSTB	Reset Input, active low
MODE	Mode Selection: 1—I2C, pull-down after POR
SCSB	Wakeup from SLEEP state
SCL	I2C Clock Input
SDA	I2C Data I/O
A4	I2C Address Bit 4

10.2 I2C Supported Feature

I2C Slave Mode Optional	Support or Not
Standard-mode – 100 kbps	Yes
Fast-mode – 400 kbps	Yes
Fast-mode Plus – 1000 kbps	Yes
High-speed mode – 3200 kbps	No
Clock Stretching	No
10-bit slave address	No
general call address	No
software reset	No
device ID	No

10.3 I2C Command Format

Example I2C Data Transfers:

Master writes 1 or more data bytes to PL1166 FIFO register:

| Start | Device_Addr[6:0] | W | A | Byte_Addr[7:0] | A | Data[7:0] | A | — — — — | A | Data[7:0] | A | Stop |

Master writes 1 byte to PL1166 to specify FIFO register, then reads one or more bytes from PL1166 FIFO:

| Start | Device_Addr[6:0] | W | A | Byte_Addr[7:0] | A | Sr | Device_Addr[6:0] | R | A | Data[7:0] | A | | A | Data[7:0] | NA | Stop |

Master may continue reading PL1166 FIFO:

| Start | Device_Addr[6:0] | R | A | Data[7:0] | A | Data[7:0] | A | — | A | Data[7:0] | NA | Stop |

Sr: repeated Start

A: Acknowledge   NA: No acknowledge   Master to Slave   Slave to Master

10.4 I2C Device Address

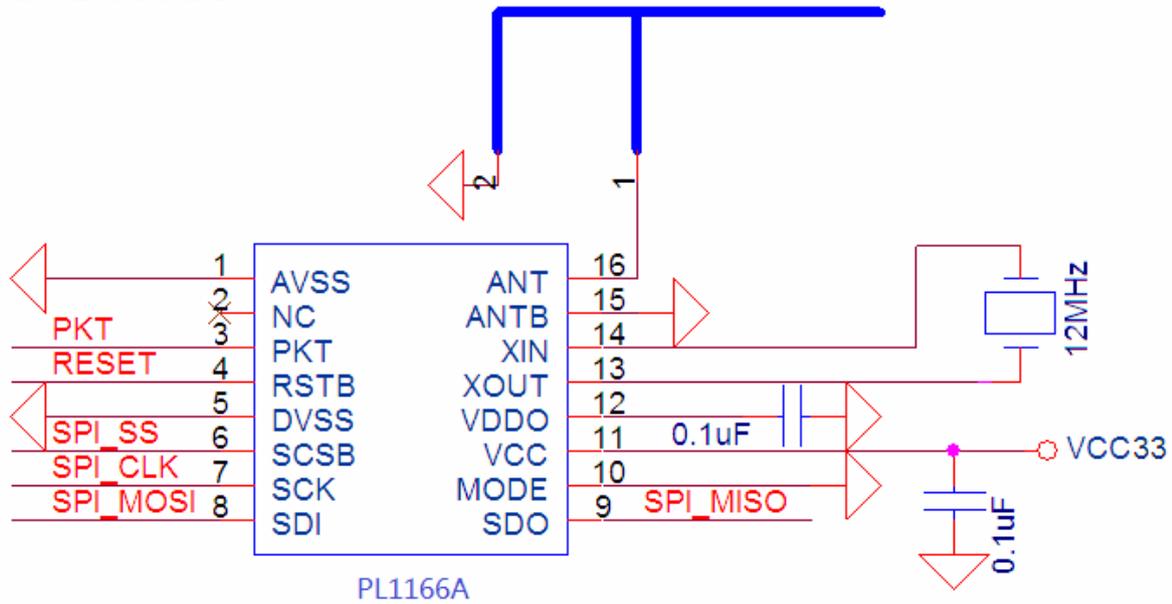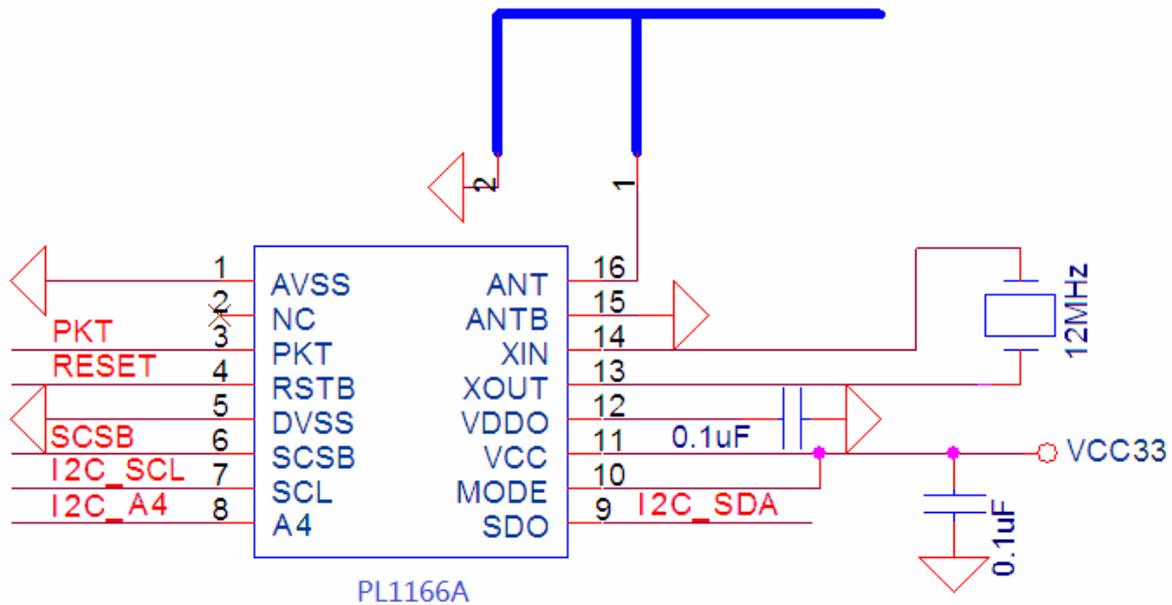| A6	A5	A4	A3	A2	A1	A0	R/W
0	1	A4 Pin	1	0	0	0	Read=1 Write=0

11 Control Register Information

The latest recommended control registers value is in user manual, please contact with POWERLINK.

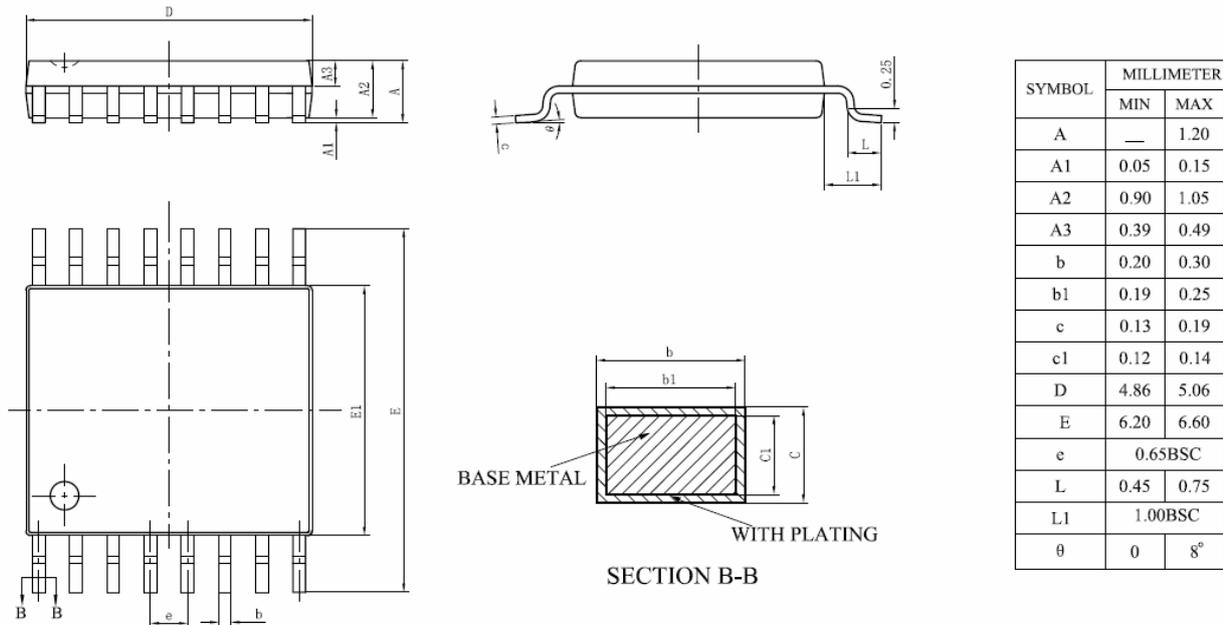# 12 Typical Application

SPI Mode
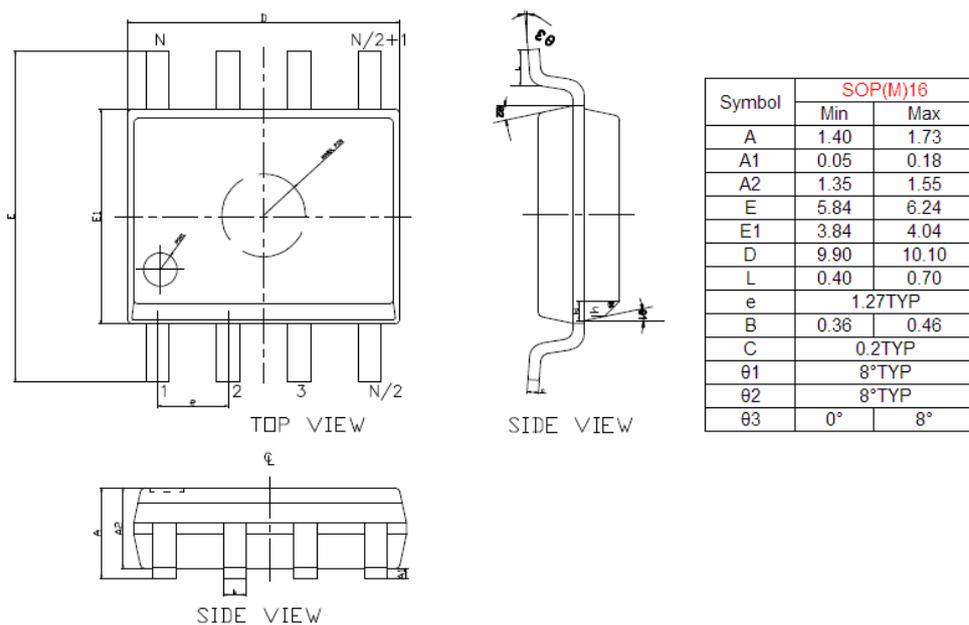

PL1166A

I2C Mode

PL1166A

13 Packaging Information

TSSOP16 package

TSSOP16 PACKAGE OUTLINE DIMENSIONS

SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°

BASE METAL

WITH PLATING

SECTION B-B

SOP16 package

SOP16 PACKAGE OUTLINE DIMENSIONS

Symbol	SOP(M)16	
	Min	Max
A	1.40	1.73
A1	0.05	0.18
A2	1.35	1.55
E	5.84	6.24
E1	3.84	4.04
D	9.90	10.10
L	0.40	0.70
e	1.27TYP	
B	0.36	0.46
C	0.2TYP	
θ1	8°TYP	
θ2	8°TYP	
θ3	0°	8°

TOP VIEW

SIDE VIEW

SIDE VIEW

14 Document Revision History

Rev.	Date	Comments
0.2	2015/12/18	Preliminary Version
1.0	2016/11/07	Formal release Version：TSSOP16/SOP16 1) Added SPI note to 9.2 SPI command format 2) Fixed 10.3 I2C command format figure 3) Fixed f_{OP} Parameter: 2402~2480
1.1	2018/07/11	Operating Temperature

15 Important Notice

POWERLINK reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.